AMENDMENTS TO THE SUBSTITUTE SPECIFICATION:

Please replace the paragraph on page 11, beginning on line 19 thereof, with the following amended paragraph:

Then, metallic layer 104 is made to react with polycrystalline silicon layer 103 by heat treatment at 650°C or higher in a process for forming a CMOS device, thereby forming metal silicide layer 108 of e.g. tungsten ~~suicide~~ silicide to a thickness about twice as large as that of deposited metallic layer 104.

Please replace the paragraph beginning on page 15, line 18, and bridging to page 16, line 15, with the following amended paragraph:

Then, gate insulation layer 310 is formed on the surface of semiconductor substrate 301 e.g. by thermal oxidation, and polycrystalline silicon layer is formed thereon e.g. by CVD. The polycrystalline silicon layer is locally doped with an impurity of n-type (e.g. phosphorus) and with another impurity of p-type (e.g. boron) by ion implanting, thereby forming n-type polycrystalline silicon layer 311 as an NMOS gate electrode and p-type polycrystalline silicon layer 312 as a PMOS gate electrode, respectively, followed by activation annealing at 950°C. Then, metallic layer 309 of e.g. tungsten is deposited thereon to a thickness of about 5 nm e.g. by sputtering, where precleaning e.g. with hydrofluoric acid is carried out beforehand to remove natural oxide. etc. remaining on the surfaces of polycrystalline silicon layers 311 and 312. Then, metal nitride layer 308 of e.g. tungsten nitride as a reaction barrier and metallic layer 307 of e.g. tungsten are deposited thereon one after the other to a thickness of ~~about 5 to about~~ about 5 to about 10 nm and to a thickness of about 50 nm, respectively, e.g. by sputtering. It is desirable to deposit these metallic layer 309, metal nitride layer 308 and metallic layer 307 continuously without exposing to the air. Then, silicon oxide layer 306 is deposited on metallic layer 307 e.g. by plasma CVD.